What is claimed is:

1. A semiconductor memory device, comprising:

a cell array having a plurality of cells;

a plurality of bit lines supplied with voltage stored in the plurality of the cells;

a plurality of sense amplifier means for sensing and amplifying a voltage of the plurality of the bit lines, each bit line being connected to each cell;

a plurality of switches for selectively connecting or disconnecting the plurality of the sense amplifier means to the plurality of the bit lines; and

a sense amplifier control means for turning on the plurality of the switches by using at least two different timing sets.

2. A semiconductor memory device, comprising:

a cell array having a plurality of cells;

a plurality of sense amplifier means for sensing and amplifying a voltage of a plurality of bit lines, each bit line being connected to each cell;

a plurality of switches for connecting or disconnecting the plurality of the sense amplifier means to the plurality of the bit lines;

a sense amplifier control means for outputting a control signal for turning on the plurality of the switches;

a wire for transmitting the control signal to the sense

amplifier control means; and

a delay means for delaying the control signal for a predetermined time, the delay means being inserted into wire.

3. The semiconductor memory device as recited in claim 2, wherein the delay means outputs one signal delayed for a predetermined time from the control signal.

4. The semiconductor memory device as recited in claim 1, wherein the switch includes a MOS transistor.

5. The semiconductor memory device as recited in claim 3, wherein the delay means includes a resistance.

6. The semiconductor memory device as recited in claim 3, wherein the delay means includes a serially connected inverter.

7. The semiconductor memory device as recited in claim 3, wherein the delay means generates a plurality of enable signals orderly delayed for a predetermined time interval from the control signal, and the plurality of the enable signals orderly turn on the plurality of the sense amplifier means.

8. The semiconductor memory device as recited in claim 7, wherein the plurality of the enable signals orderly delayed are generated by using a serially connected resistance.

9. The semiconductor memory device as recited in claim 7, wherein a plurality of the enable signals orderly delayed are generated by using several serially connected inverters.

10. A semiconductor memory device, comprising:

a cell array having a plurality of cells;

a plurality of bit lines supplied with voltage stored in the plurality of the cells;

a plurality of sense amplifier means for sensing and amplifying a voltage of the plurality of the bit lines;

a plurality of switches for connecting or disconnecting the plurality of the sense amplifier means to a plurality of the bit lines;

a first sense amplifier control means for turning on one part of the plurality of the switches in a first timing set; and

a second sense amplifier control means for turning on the other part of the plurality of the switches in a second timing set, the other part not being turned on in the first timing set.

11. The semiconductor memory device as recited in claim 10, further comprising:

a plurality of a first delay means serially connected for orderly turning on the one part of the plurality of the switches mandated to be turned on in the first timing set; and

a plurality of a second delay means serially connected

for orderly turning on the other part of the plurality of the switches mandated to be turned on in the second timing set.

12. The semiconductor memory device as recited in claim 11, wherein the second sense amplifier control means is controlled by a signal delayed through the use of a control signal that controls the first sense amplifier control means.

13. The semiconductor memory device as recited in claim 10, wherein the switch includes a MOS transistor.